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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/542,783 | 04/04/2000 | John Whitman | 4294US(98-1208) | 6870 |

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|---|---|
| KEBEDE, BROOK | |
| ART UNIT | PAPER NUMBER |
| 2823 | |

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/542,783 | Applicant(s) WHITMAN ET AL. | |
|---|---|---|---|
| | Examiner Brook Kebede | Art Unit 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is less than three months from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) *18-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. Applicants' request regarding the entry of preliminary amendment that was mailed on January 31, 2001 is acknowledged.

The Office has received a fax copy of the preliminary amendment and substitute specification on October 5, 2001 with certificate of mailing that was dated January 31, 2001. This preliminary amendment has been considered by the Examiner and entered in Paper No. 7. The Office actions, i.e., Office actions in Paper No. 8 and 9 are based on the preliminary amendment that was resubmitted on October 5, 2001 in Paper No. 7.

2. Applicants' change of election of Species I form ***with traverse*** to ***without traverse*** of Paper No. 8 is acknowledged. As of record, the election of Paper No. 8. should stand as follow:

a. Applicants' election without traverse of Group I (Claims 1-87) in Paper No. 8 is acknowledged.

b. Applicants' election change form *with traverse* to *without traverse* of Species I (Claims 1-17) in Paper No. 11 is acknowledged.

c. Claims 88-101 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

d. Claims 60-87 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

e. Claims 18-59 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 11.

***Drawings***

3. The formal drawings were received on May 28, 2002 in Paper No. 10. These drawings are acceptable.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, 8, 9, 11, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi et al. (US/6,278,153).

*The rejection that was set forth in Paper No. 9 is maintained and repeated herein below as of record.*

Re claim l, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of said at least one recess (23a) without subsequently removing the material (20) from over the surface (23 24 25 26) (see Figs. 6A-6D; 10A-10E and 13A-13E; ).

Re claim 2, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including disposing the material so as to substantially fill the at least one recess without substantially covering said surface (see Figs. 6A-6D; 10A-10E and 13A-13E; ).

Re claim 8, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess (see Figs. 6A-6D; 10A-10E and 13A-13E).

Re claim 9, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material (see Figs. 6A-6D; 10A-10E; 13A-13E)

Re claim 11 as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said semiconductor device structure (see Fig. 6A-6D; 10A-10E; 13A-13E).

Re claims 16 and 17, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material, with a non-planar surface disposed in said at least one dual damascene trench add at least partially covering sand surface and disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing (see Figs. 14A-14D).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Yoshihara (US/6,117,486).

Re claims 3-7, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure (see Kikuchi et al. Figs. 6A-6D; 10A-10E and 13A-13E). However, Kikuchi et al. do not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature ; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Lin et al. (US/6,046,083).

Re claim 10, as applied to claim 9 above, Kikuchi et al. disclose all the claimed limitations including forming of stacked capacitor structure having conductive layer. Although it is well-known in the art Kikuchi et al. do not disclose doped HSG.

Lin et al. disclose providing said semiconductor device structure having a stacked capacitor structure with the surface and at least one container being lined, with doped hemispherical grain polysilicon (see Figs. 7 and 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with doped HSG as taught by Lin et al. because the device performance would have been enhanced (see Lin et al. Col. 1, lines 59-67 through Col. 2, lines 1-14).

9. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Park et al. (US/6,326,282).

Re claim 12, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation except providing a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

Park et al. disclose forming of a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure in order to form an isolation region between the device elements (see Figs. 2B-2E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with

shallow trench isolation structure as taught by Park et al. because the shallow trench isolation structure would have provided isolation region between device elements in the substrate.

Re claim 13, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure (see Park et al. Figs. 2B-2E).

Re claim 14, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface see Park et al. Figs. 2B-2E).

Re claim 15, as applied to claim 14 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing see Park et al. Figs. 2B-2E).

***Response to Arguments***

10. Applicant's arguments filed on May 28, 2002 in Paper No. 11 have been fully considered but they are not persuasive.

Regarding claim rejection of claims 1, 2, 8, 9, 11, 16, and 17 under 35 U.S.C. § 102(e) applicants argued that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal

Brothers v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Kikuchi describes a process for forming a thin-film capacitor. Among other things, and with reference to the example provided in FIGS. 6A-6I of Kikuchi, the process of Kikuchi includes providing a fabrication substrate 21, forming electrodes 22 on a surface of the fabrication substrate 22, and applying a layer 23 of dielectric material over the fabrication substrate 21 and the electrodes 22 thereon. As described, the layer 23 of dielectric material is formed by coating a negative type epoxy acrylate resin onto a surface of the fabrication substrate 21 at a thickness of about 10 microns. Col. 18, line 59, to col. 19, line 4. Recesses 23a are formed in layer 23, over electrodes 22 therebeneath to define capacitor containers. As each recess 23a is formed over an electrode, the depth thereof is less than the 10 micron thickness of the layer 23 of dielectric material. After appropriate capacitor electrode and dielectric layers have been formed, a photoresist 20 is applied to the resulting structure. As shown in various Figures of Kikuchi, including FIGs. 6D, l OC, and 13D, the photoresist 20 (photoresist 126 in FIG. IOC and photoresist 155 in FIG. 13D) substantially fills each of the recesses 23a. Although regions of the photoresist 20 that are located over the surface of layer 23 appear in the Figures of Kikuchi to be thinner than the depths of the recesses 23a, Kikuchi quite clearly explains, for example, at col. 20, lines 13-24, that the photoresist is coated onto the structure so as to have a thickness of about 10 microns, which is greater than the depths of the recesses 23 a. Independent claim 1 of the above-referenced application recites a method for disposing a material on a semiconductor device structure. The method of claim 1 includes providing a semiconductor device structure with a surface and at least one recess formed in the

surface, as well as disposing material on the surface "so as to substantially fill [the] at least one recess" and such that material covering the surface has "a thickness less than a depth of [the] at least one recess without subsequently removing the material from over [the] surface." As Kikuchi describes a method that includes application of photoresist 23 so as to substantially fill recesses that are less than 10 microns deep and so as to have a thickness of about 10 microns over the surface of a fabrication substrate, it is respectfully submitted that Kikuchi neither expressly nor inherently describes "disposing material . . . so as to substantially fill . . . at least one recess . . . " while material covering the surface of the fabrication substrate has "as thickness less than a depth of [the] at least one recess . . .", as recited in claim 1. It is, therefore, respectfully submitted that Kikuchi does not anticipate each and every element of claim 1. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), claim 1 is allowable over Kikuchi. Each of claims 2, 8, 9, 11, 16, and 17 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. Claim 2 is additionally allowable since Kikuchi does not expressly or inherently describe disposing material so as to substantially fill at least one recess of a semiconductor device structure with material without substantially covering a surface of the semiconductor device structure with the material, and doing so "without subsequently removing material from over [the] surface" (claim 1). The description of Kikuchi is limited to forming a layer of photoresist to substantially fill a recess 23a which has a depth of less than 10 microns with a material with the material over surfaces of an intermediate structure in which the recess is formed having a thickness of about 10 microns. The intermediate structure of Kikuchi does not have the elements recited in claim 2 until after material has been removed from the surface thereof. Claim 17 depends from claim 16 and is also

allowable since Kikuchi neither expressly nor inherently describes disposing a stress buffer over a layer of conductive material such that the stress buffer has a substantially planar surface without removing material thereof following disposition thereof. For these reasons, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 be withdrawn."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The rejected claims under 35 U.S.C. § 102(e) are anticipated by Kikuchi et al. '153 as applied in Paragraph No. 5 herein above. In addition, Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Furthermore, the claims as recited in claim 1 does not specifically call for a particular semiconductor device and the preamble recites "a method deposing a material on a semiconductor device structure comprising..." and the body of the claim also does not provide a positive or negative recitation that identified a particular semiconductor device. For this reason applicants argument that, *Kikuchi describes a process for forming a thin-film capacitor. Among other things, and with reference to the example provided in FIGS. 6A-6I of Kikuchi, the process of Kikuchi includes providing a fabrication substrate 21, forming electrodes 22 on a surface of the fabrication substrate 22, and applying a layer 23 of dielectric material over the fabrication substrate 21 and the electrodes 22 thereon. As described, the layer 23 of*

*dielectric material is formed by coating a negative type epoxy acrylate resin onto a surface of the fabrication substrate 21 at a thickness of about 10 microns. Col. 18, line 59, to col. 19, line 4. Recesses 23a are formed in layer 23, over electrodes 22 therebeneath to define capacitor containers. As each recess 23a is formed over an electrode, the depth thereof is less than the 10 micron thickness of the layer 23 of dielectric material. After appropriate capacitor electrode and dielectric layers have been formed, a photoresist 20 is applied to the resulting structure. As shown in various Figures of Kikuchi, including FIGs. 6D, l OC, and 13D, the photoresist 20 (photoresist 126 in FIG. IOC and photoresist 155 in FIG. 13D) substantially fills each of the recesses 23a. Although regions of the photoresist 20 that are located over the surface of layer 23 appear in the Figures of Kikuchi to be thinner than the depths of the recesses 23a, Kikuchi quite clearly explains, for example, at col. 20, lines 13-24, that the photoresist is coated onto the structure so as to have a thickness of about 10 microns, which is greater than the depths of the recesses 23 a. Independent claim 1 of the above-referenced application recites a method for disposing a material on a semiconductor device structure. The method of claim 1 includes providing a semiconductor device structure with a surface and at least one recess formed in the surface, as well as disposing material on the surface "so as to substantially fill [the] at least one recess" and such that material covering the surface has "a thickness less than a depth of [the] at least one recess without subsequently removing the material from over [the] surface." As Kikuchi describes a method that includes application of photoresist 23 so as to substantially fill recesses that are less than 10 microns deep and so as to have a thickness of about 10 microns over the surface of a fabrication substrate, it is respectfully submitted that Kikuchi neither expressly nor inherently describes "disposing material . . . so as to substantially fill . . . at least*

*one recess . . . " while material covering the surface of the fabrication substrate has "as thickness less than a depth of [the] at least one recess . . .", as recited in claim 1. It is, therefore, respectfully submitted that Kikuchi does not anticipate each and every element of claim 1*, does not have merit since the recited claimed invention is within the scope of Kikuchi et al. '153, i.e., method of disposing a material on a semiconductor device structure is disclosed. Further, applicants argument is so confusing because in one hand applicants arguing that Kikuchi et al. does not teach the claimed limitation on the other hand applicants are admittedly pointed out " *Kikuchi describes a method that includes application of photoresist 23 so as to substantially fill recesses.* " The "material" recited in the rejected claims is a resist material and the "device" recited in the rejected claims is a "semiconductor device structure" and all these are disclosed by Kikuchi et al. '153. In addition, the limitation, "the material covering the surface having thickness less than the depth of said at least one recess without subsequently removing the material form the surface," is disclosed by Kikuchi et al. '153 (see Fig. 6D). Finally, the Examiner respectfully would like to point out there is no physical measurement with respect to the depth of the recess and the thickness of the material that disposed on the surface in the rejected claims. In the absence showing clear and distinguishable difference between the prior art and instant application claimed invention, the Examiner respectfully submits that applicants argument is not commensurate with the scope of the claims, in particularly, as stated above. Therefore, the rejection under 35 U.S.C. § 102(e) is deemed proper.

Regarding claim rejection of claims 3-7under 35 U.S.C. § 103(a), applicants argued that "Claims 3-7 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. A summary of the teachings of Kikuchi is provided above.

Yoshihara teaches a resist coating method that includes applying resist to a substrate as the substrate is being rotated, decreasing the rate of rotation of the substrate for a predetermined period of time, and re-increasing the rate at which the substrate is rotated. Yoshihara does not, however, teach or suggest that re-increasing of the rate of spinning of the substrate is effected gradually, as recited in claim 3. Rather, Yoshihara merely teaches and suggests that the rate of spinning is re-increased. As is known in the art, spinning of a substrate may be effected very quickly, and need not be effected gradually. Kikuchi likewise lacks any such teaching or suggestion. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 3 is allowable over the combination of Kikuchi and Yoshihara. For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 3-7 be withdrawn."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Kikuchi et al. 153' and Yoshihara '486 as applied in Paragraph 7 herein above.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claim 10 under 35 U.S.C. § 103(a), applicants argued that "Claim 10 is allowable, among other reasons, as depending from claim 1, which is allowable."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Kikuchi et al. 153' and Lin et al '083 as applied in Paragraph 8 herein above.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claims 12-15, under 35 U.S.C. § 103(a), the applicants argued that "claims 12-15 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. Kikuchi teaches a method for forming a thin-film capacitor of a wiring board. Park teaches a method for forming shallow trench isolation structures in semiconductor substrates. It is respectfully submitted that, without the benefit of hindsight provided by the above-referenced application, one of ordinary skill in the art would not have been motivated to combine the teachings of Kikuchi and Park in the manner that has been asserted. This is because of the diversity between the methods and the resulting structures taught in Kikuchi and Park. In particular, Kikuchi teaches methods for forming thin-film capacitors. as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park"). Claims 12-15 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. Kikuchi teaches a method for forming a thin-film capacitor of a wiring board. Park teaches a method for forming shallow trench isolation structures in semiconductor substrates. It is respectfully submitted that, without the benefit of hindsight provided by the above-referenced application, one of ordinary skill in the art would not have been motivated to combine the teachings of Kikuchi and Park in the manner that has been asserted. This is because of the diversity between the methods and the resulting structures taught in Kikuchi and Park. In particular, Kikuchi teaches methods for forming thin-film capacitors. The thin-film capacitors of Kikuchi are not part of a semiconductor device structure but, rather, are a part of a wiring board."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above.

The combination of Kikuchi et al. 153' and Park et al. '282 as applied in Paragraph 9 herein above. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

***Conclusion***

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Correspondence***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
August 11, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800